VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claims 1 and 10 have been amended as follows:

1. (Amended three times) An integrated circuit having logic blocks comprising

a control unit for performing test and debug operations of said logic blocks of said integrated circuit;

a memory associated with said control unit, said memory holding instructions for said control unit; and

a plurality of probe lines responsive to said control unit for carrying system operation signals [at] from predetermined probe points of said logic blocks, wherein said probe lines comprise strings of storage elements providing signal paths [between] from said probe points [and] to said memory, said signal paths capable of moving sets of said system operation signals at system operation clock rates, said sets of system operation signals stored in said memory so that said sets of system operation signals are retrievable.

10. (Amended three times) An integrated circuit comprising

an interface for coupling to an external diagnostic processor;

a unit responsive to instructions from said external diagnostic processor for capturing sets of sequential system operation signals of said integrated circuit;

a plurality of probe lines coupled to said unit for carrying said system operation signals [at] from predetermined probe points of said integrated circuit, wherein said probe lines comprise strings of storage elements providing signal paths [between] from said probe points [and] to said unit, said signal paths capable of moving said sets of sequential system operation signals at system operation clock rates;

a memory coupled to said unit and to said interface, said sets of sequential system operation signals stored in said memory at one or more clock signal rates internal to said integrated circuit and retrieved from said memory through said interface to said external process at one or more clock signal rates external to said integrated circuit so that said external diagnostics processor can process said captured system operation signals.

15. (Amended three times) A method of operating an integrated circuit having logic blocks, a control unit, a memory and a plurality of probe lines of said logic blocks, said method comprising

operating said logic blocks to perform normal system operations at one or more system clock signal rates internal to said integrated circuit to produce sets of system operation signals;

enabling said probe lines responsive to said control unit to capture and carry said sets of system operation signals of said logic blocks at said system clock signal rates internal to said integrated circuit;

retrieving said sets of system operation signals from said logic blocks along said probe lines at said system clock signal rates internal to said integrated circuit,

storing said sets of system operation signals in said memory at said system clock signal rates internal to said integrated circuit; and

processing said sets of stored system operation signals to perform test and debug operations of said logic blocks of said integrated circuit.